What is claimed is:

1. A semiconductor device comprising:

a support substrate;

an insulation layer on top of the support substrate;

an SOI layer formed on top of the insulation layer;

at least one element formed on the SOI layer; and

at least one groove formed in the support substrate, the at least one groove being located below a target element whose dielectric loss is to be controlled among the at least one element.

2. The semiconductor device according to claim 1, wherein the at least one groove is formed such that a reverse face of the insulation layer is exposed.

3. The semiconductor device according to claim 1, wherein the at least one element is an analog element.

4. The semiconductor device according to claim 3, wherein the analog element is an inductor.

5. The semiconductor device according to claim 1, wherein the support substrate is one of a silicon substrate and a sapphire substrate.

6. A semiconductor device comprising:

a support substrate;

an insulation layer formed on the support substrate;

an SOI layer formed on the insulation layer;

a plurality of analog elements formed on the SOI layer;

at least one groove formed in the support substrate such that the at least one groove is located below one or more target

elements among the plurality of analog elements.

7. The semiconductor device according to claim 6, wherein the groove is formed such that a reverse face of the insulation layer is exposed.

8. The semiconductor device according to claim 6, wherein the one or more target elements are inductors.

9. The semiconductor device according to claim 6, wherein the target element is an element for which control of the dielectric loss is sought, among the plurality of analog elements.

10. The semiconductor device according to claim 6, wherein the support substrate is one of a silicon substrate and a sapphire substrate.